ACS APPLIED MATERIALS & INTERFACES

Article

Probing Interface Defects in Top-Gated MoS Transistors with Impedance Spectroscopy

Peng Zhao, Angelica Azcatl, Yuri Y Gomeniuk, Pavel Bolshakov, Michael Schmidt, Stephen J McDonnell, Christopher L Hinkle, Paul K. Hurley, Robert M. Wallace, and Chadwin Young

ACS Appl. Mater. Interfaces, **Just Accepted Manuscript** • DOI: 10.1021/acsami.7b06204 • Publication Date (Web): 26 Jun 2017

ACS Publications

ACS Applied Materials & Interfaces is published by the American Chemical Society. 1155 Sixteenth Street N.W., Washington, DC 20036

Probing Interface Defects in Top-Gated MoS_2 Transistors with Impedance Spectroscopy

Peng Zhao,[1] Angelica Azcatl,[1] Yuri Y. Gomeniuk,,[2, 3] Pavel Bolshakov,[1] Michael Schmidt,[2] Stephen J. McDonnell,[4] Christopher L. Hinkle,[1] Paul K. Hurley,[2] Robert M. Wallace,[1] and Chadwin D. Young[*, 1]*

[1] Department of Materials Science and Engineering, The University of Texas at Dallas, 800 W Campbell Rd, Richardson, TX 75080, USA

[2] Tyndall National Institute, Department of Chemistry, University of College Cork, Lee Maltings, Dyke Parade, Cork, Ireland

[3] V. Lashkaryov Institute of Semiconductor Physics, NAS of Ukraine, 41, pr. Nauki, Kyiv, Ukraine

[4] Department of Materials Science and Engineering, The University of Virginia, Charlottesville, VA, USA

Abstract The electronic properties of the HfO_2/MoS_2 interface were investigated using multi-frequency capacitance-voltage (C-V) and current-voltage characterization of top-gated MoS_2 metal-oxide-semiconductor field effect transistors (MOSFETs). The analysis was performed on few layer (5 - 10) MoS_2 MOSFETs fabricated using photolithographic patterning with 13 nm and 8 nm HfO_2 gate oxide layers formed by atomic layer deposition after in-situ UV-O_3 surface functionalization. The impedance response of the HfO_2/MoS_2 gate stack indicates the existence of specific defects at the interface, which exhibited either a frequency dependent distortion similar to conventional Si MOSFETs with unpassivated silicon dangling bonds, or a frequency dispersion over the entire voltage range corresponding to depletion of the HfO_2/MoS_2 surface,

consistent with interface traps distributed over a range of energy levels. The interface defects density (D_{it}) was extracted from the C-V responses by the high-low frequency and the multiple-frequency extraction methods, where a D_{it} peak value of 1.2×10^{13} cm^{-2} eV^{-1} was extracted for a device (7-L MoS_2 and 13 nm HfO_2) exhibiting a behavior approximating to a single trap response. The MoS_2 MOSFET with 4-L MoS_2 and 8 nm HfO_2 gave D_{it} values ranging from 2×10^{11} cm^{-2} eV^{-1} to 2×10^{13} cm^{-2} eV^{-1} across the energy range corresponding to depletion near the HfO_2/MoS_2 interface. The gate current was below 10^{-7} A/cm^2 across the full bias sweep for both samples indicating continuous HfO_2 films resulting from the combined UV ozone and HfO_2 deposition process. The results demonstrated that impedance spectroscopy applied to relatively simple top-gated transistor test structures provides an approach to investigate electrically active defects at the HfO_2/MoS_2 interface and should be applicable to alternative TMD materials, surface treatments and gate oxides as an interface defect metrology tool in the development of TMD-based MOSFETs.

Keywords Molybdenum disulfide (MoS_2), high-*k* dielectrics, interface defects, electrical characterization, top-gated transistors, capacitance – voltage (C-V).

Introduction

Over the past decade, two-dimensional (2-D) materials have attracted considerable attention due to their atomically-thin structure and their unique electronic, optical and mechanical properties [1–3]. Among these materials, transition metal dichalcogenides (TMDs) have demonstrated satisfactory energy bandgap values and promising properties for future applications in electronics and optoelectronics [4–17]. Molybdenum disulfide (MoS_2), as the most explored TMD material, has been reported to exhibit an electron mobility of 55 cm^2 / V·s in a top-gated transistor with a single layer of MoS_2 [4–6], and a theoretical value of 410 cm^2 / V·s at room temperature [7]. Moreover, compared with monolayer MoS_2, few-layer MoS_2 has been predicted and experimentally demonstrated as an excellent channel material to achieve high mobility and reduced contact resistivity [8–12]. With the ultimate electrostatic control due to the 2-D structure, an energy gap in the range of 1.2eV to 1.8eV, and the high mobility value, MoS_2 is especially attractive for high performance, low power-consumption flexible electronics [1,10,18,19].

As the utilization of high dielectric constant (high-*k*) gate oxide material in conventional silicon CMOS processing has been demonstrated to reduce the gate leakage and enable further scaling of transistors, high-*k* dielectrics are also considered extensively for TMD transistors [5,10,11,16,18–28]. In addition, high-*k* materials can suppress the coulombic scattering in low dimensional nanostructures, increasing the carrier mobility, as shown in the literature with both theoretical simulation [20] and experimental evidence [5,11]. Although back gated structures are ideal for contact and doping research on TMD transistors [8,29,30], top gate devices are more attractive for integrated circuit manufacturing. Thus, investigating high-*k* deposition on TMDs and understanding the interface properties is an important scientific and technological research area.

An obstacle of integrating high-*k* dielectrics on these 2-D materials is the lack of bonds available at the surface that enables thin film deposition [21,22]. Many top-gated transistors in the literature adopted thick gate dielectric deposition, usually from 15 nm to 50 nm [5,11,16,23], to avoid pin holes and non-uniformity in the dielectric. Recently, multiple surface functionalization methodologies have been reported for thin, uniform high-k dielectric deposition on MoS_2 [22,24–27]. Metal seed layers [24], oxygen plasma treatment [22,25] and ultraviolet-ozone ($UV\text{-}O_3$) treatment [26,27] are promising pre-deposition approaches to gain a uniform dielectric layer. However, since the ultimate goal of these approaches is the enhancement of electronic device performance, detailed reports on device performance related to the impacts of these treatments is vital, but only shown in a few papers [24,25,31]. Our previous research suggested that defects existed at the high-k/MoS_2 interface region after an ex-situ UV-O_3 treatment [28], but the gate oxide leakage on these large area MOS structures affected the analysis, due to the rough surface of the bulk MoS_2 sample and relatively large capacitor area. Recently, Azcatl et al., [26,27] reported that the non-destructive (i.e., no Mo-oxide formation) in-situ UV-O_3 treatment featured a uniform atomic layer deposited (ALD) high-*k* oxide without unexpected interfacial layers for exfoliated MoS_2.

Impedance measurements are recognized as one of the fastest and most robust methods to investigate properties of a dielectric and its interface with the underlying substrate. However, impedance measurements of metal/high-*k* dielectric/TMD MOS system have only been reported in a limited number of works [10,11,18,31–33]. Most publications report capacitance - voltage (C-V) curves without further analysis [10,11,32], or back-gated capacitors with high-*k* deposited on Si [33]. Recently, S. Park et al.[31] reported C-V characteristics of capacitors with Al_2O_3 on 100-200 nm thick MoS_2 yielding D_{it} values of 10^{11} $cm^{-2}eV^{-1}$ to 10^{14} $cm^{-2}eV^{-1}$. For high-*k* on chemical-vapor-deposited (CVD) MoS_2 thin films, a comprehensive study of dielectric impedance was performed, showing D_{it} extraction and modeling work based on capacitors with 30 nm ALD HfO_2 on monolayer MoS_2 with 2nm Al as an interfacial seed layer[18]. Another relevant and useful D_{it} extraction work has been reported by Takenaka et al.[33], which uses the Terman method to analyze and compare interfaces of MoS_2 and SiO_2/HfO_2/Al_2O_3. The extracted D_{it} values are about 1×10^{13} $cm^{-2}eV^{-1}$ regardless of the dielectric selection for back-gated devices on semi-bulk MoS_2. However, the device architecture may not be commensurate with the necessary solution for continued device scaling where top-gated architectures dominate. Here, dielectric/substrate interfaces are dependent upon how device fabrication was executed, and therefore, should be investigated in this context.

In this work, we designed and fabricated top-gated transistors on exfoliated, few-layer MoS_2 as the test structures, with an in-situ UV-O_3 functionalization [26,27] and 8 to 13 nm ALD HfO_2, which are among the thinnest high-*k* dielectrics on top-gate TMD MOSFETs to date. As we use photolithography for source/drain and gate patterning, the gated area is sufficiently large for C-V characterization. Both transistor performance and gate-stack interface properties were characterized, with an emphasis on the impedance spectroscopy of the dielectric. The interface defect density (D_{it}) was extracted and analyzed by three different methods. Besides reporting the interface properties of our transistors, the methodology can be potentially applied to other TMDs and surface functionalization, beyond MoS_2 and UV-O_3 treatment.

Experimental Methods

The transistor structure used for the few-layer MoS_2 MOSFETs examined in this work is shown in Fig. 1a. Before device fabrication, 270nm SiO_2 was thermally grown on highly doped p-type Si wafers as a substrate. Few-layer MoS_2 flakes were mechanically exfoliated from commercially available natural MoS_2 crystals and transferred onto the SiO_2. By using conventional photolithography, we aligned a source/drain pattern on the photomask directly on the selected flake. After patterning, Au/Ti (380/20nm) was deposited as contacts in an e-beam evaporator at 2×10^{-6} Torr, followed by a lift-off process. Thereafter, a 15-minute in-situ UV-O_3 surface treatment [26] was performed. The UV-O_3 is generated based on irradiance from the fused quartz envelope, low pressure UV Hg lamp employed previously [26,27] and is estimated to be 5 mW/cm^2 which ensures no etching or Mo-oxide formation according to S. Park et al. [31] Following the UV-O_3 surface preparation, HfO_2 was deposited at 200˚C in the ALD chamber immediately after the treatment without a break in vacuum. The thermal ALD used H_2O and TDMA-Hf as the precursors, and started the deposition with a TDMA-Hf pulse. We intentionally avoided annealing the HfO_2 after deposition to study the effects of the UV-O_3 functionalization treatment and its role on HfO_2/MoS_2 interface properties without the impact of any subsequent annealing. The final step of fabrication was patterning and evaporating of Au / Cr (250/50nm) metal gate. The typical MoS_2 thickness studied in our work was about 5-10 layers (3-6 nm). The device size was determined by both lithography and the flake shape. Electrical measurements in this work were performed using a Keithley 4200 Semiconductor Characterization System and an Agilent E4980A LCR meter at room temperature (25˚C) in a shielded probe station.

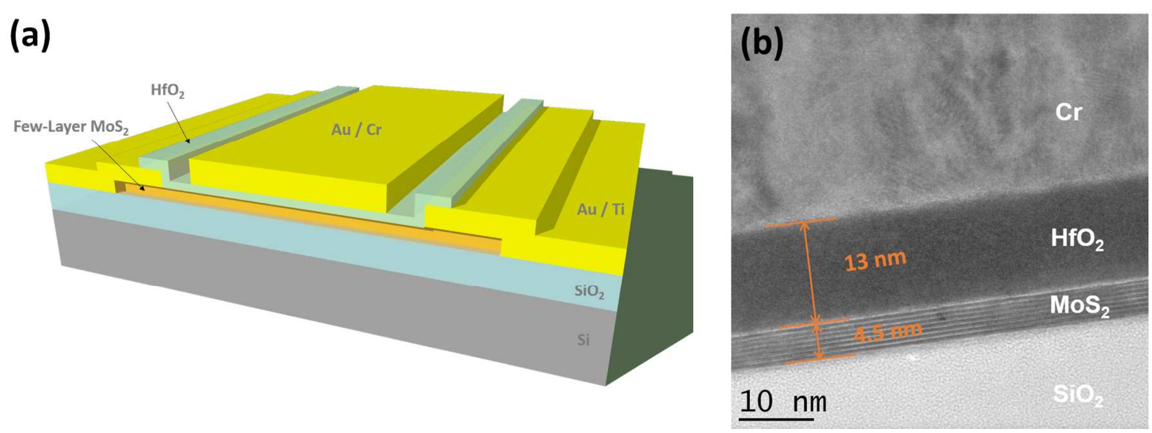


Figure 1. (a) Schematic cross section of the top-gated MoS_2 field effect transistor structure used in this work. Gate stack: Au / Cr / HfO_2 / MoS_2. (b) Cross sectional transmission electron microscopic image of the metal/HfO_2/MoS_2 transistor gate stack. 13nm HfO_2 is uniformly deposited on a 7-layer MoS_2 flake, showing no evidence of unintentional oxidation of the MoS_2 surface.

Results and Discussion

A high-resolution transmission electron microscopic (TEM) image is shown in Fig.1b, illustrating the cross section of a device gate stack with 7 layer MoS_2 and a 13 nm HfO_2 dielectric. The active channel length under the metal gate is 6.5 μm and the channel width is 9.5 μm. Fig. 2a shows the I_{DS}-V_{GS} and the gate leakage characteristics for this MoS_2 transistor. V_{DS} was kept at 0.5V. An excellent on/off ratio of 10^6 was observed, with an ultra-low leakage current on the gate. The MoS_2 was intrinsically n-type doped, consistent with our previous observation [28] and literature reports [5,8,24,29]. The relatively large negative threshold voltage (V_T = -3V) is possibility due to the fixed positive charge in the dielectric layer(s). Similar large $|V_T|$ was also observed by other researchers using top-gated MoS_2 transistors with high-*k* dielectrics[11,24]. Since the HfO_2 is deposited at low temperature (200 °C) with no post deposition annealing (to assess the UV-O_3 treatment without convolution from additional annealing), a possible net oxide charge being present in the HfO_2 layer may result. Furthermore, possible contribution of induced charges in the underlying SiO_2 from potential x-rays exposure during the electron beam deposition process – which was used to form the metal gate and source/drain regions – could occur. Thus, both oxide layers could possess trapped charge. Assuming the threshold voltage shift ΔV=-3V originates from oxide charges, the density of the positive fixed charges can be estimated by $Q_f / q = - C_{ox} \cdot \Delta V / q = 1.4\times10^{13}\ /cm^2$. Fig. 2b shows the I_{DS}-V_{DS} curves with V_{GS} swept from -4 V to 0 V. A non-linear region was observed at low V_{DS}, likely because of high resistance Schottky barriers at the source/drain contacts associated with this unannealed device [5,34]. This is expected, as there is no intentional doping in the MoS_2 film in the source and drain region. As is the case in conventional 3D semiconductors, increasing the doping in the MoS_2 film to high concentrations (> $1x10^{19}$ cm^{-3}), for example via Nb doping [35], significantly reduces the specific contact resistivity at the Ti/MoS_2 interface. In addition, it is noted from Fig.1a that the top-gated MOSFET has non-gated regions between the gate edge and the source and drain contacts (approximately 1-2μm on each side), which is another source of series resistance in the structure.

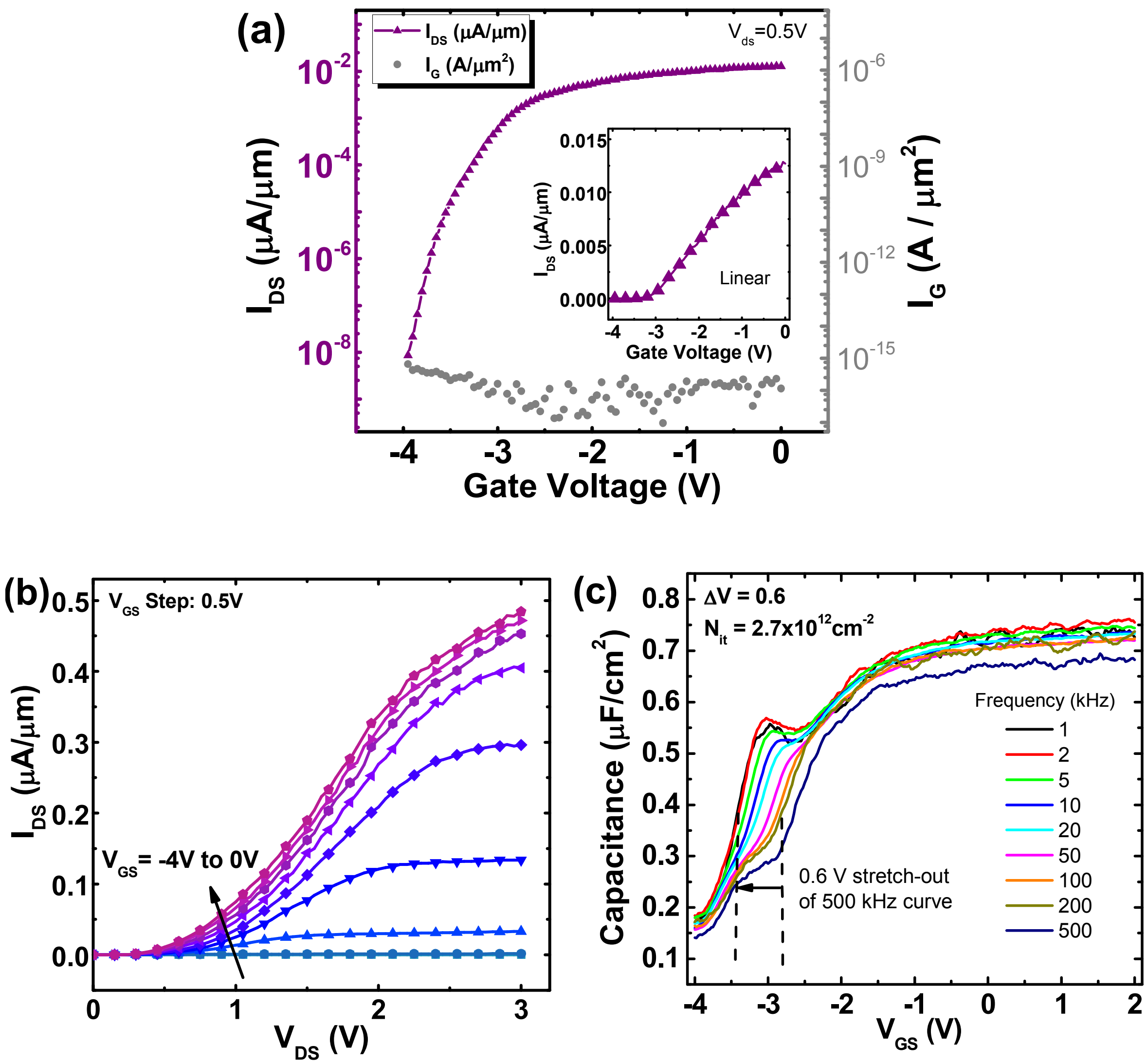


Figure 2. Electrical characterization of device with 13 nm HfO_2 and 7-layer MoS_2 (L=6.5μm,W=9.5μm). (a) I_{DS} - V_{GS}: I_{ON} / I_{OFF} = 10^6 with ultra-low gate leakage; (b) I_{DS} – V_{DS} with V_{GS} from -4 V to 0 V; (c) C-V: frequency

dependence, where a "hump" in the range -2.5 to -3.5 V is indicating an interface defect response. The 0.6 V stretch-out of 500 kHz curve indicates the Fermi energy pinning at MoS_2 / HfO_2 interface.

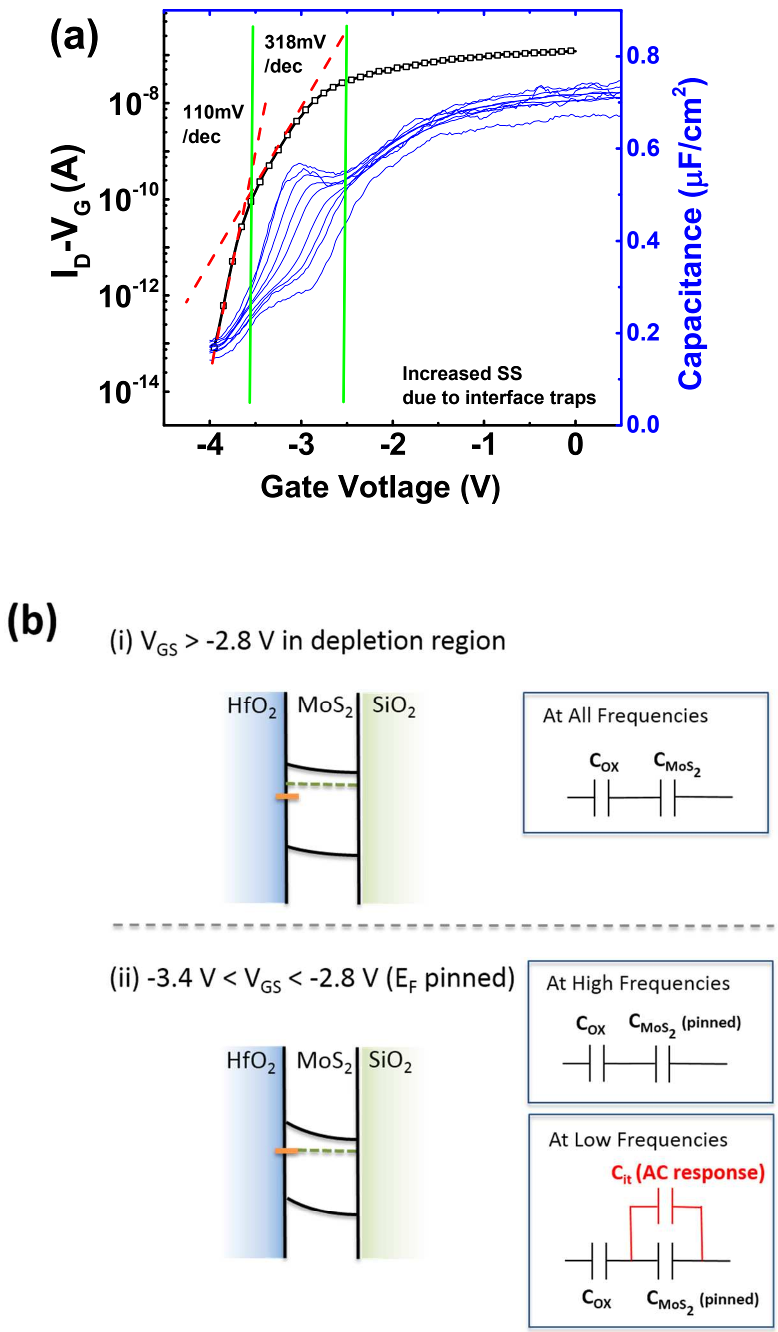


Figure 3. (a) I_D-V_G and multi-frequency C-V overlayed to illustrate the impact of D_{it} in both measurements occurs at the same Vg. SS is degraded due to interface traps and $D_{it} = 1.6 \times 10^{13}$ $cm^{-2}eV^{-1}$ is estimated. (b) Energy band diagram of high-*k* / MoS_2 interface and equivalent circuits. (i) At gate voltages higher than -2.8 V or lower than -3.4

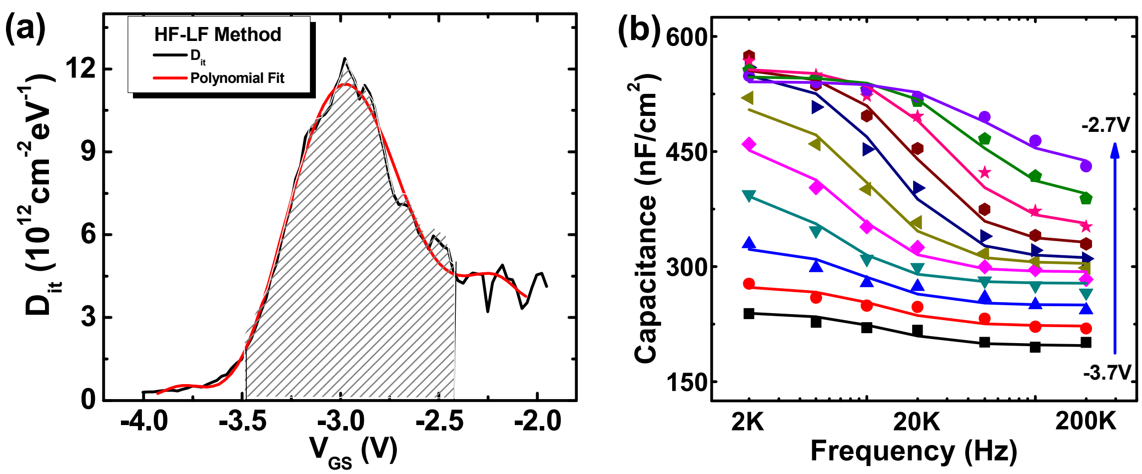
V, the total AC capacitance is due to the C_{ox} and C_{MoS2} connected in series. (ii) At gate voltage between -3.4 V and -2.8 V, the E_F is pinned at interface, and there is an AC response at low frequencies due to D_{it} but no AC response at high frequencies.

To investigate the electronic properties at HfO_2/MoS_2 interface, the source and drain were connected to one terminal of the LCR meter, while the gate is connected to the other terminal. Variable frequency C-V measurements were conducted. The back gate contact was intentionally floated to minimize the effect from oxide charge in the underlying SiO_2. The frequency dependence is shown in Fig. 2c. Since this transistor operates in accumulation mode, the reaction of the majority carriers (electrons) to the ac signal is observed. In contrast to our previous study on the ex-situ UV-O_3 treatment and bulk MoS_2 crystals [28], these C-V frequency dependence results showed a highly improved high-k/MoS_2 interface, with significantly less dispersion and lower gate leakage due to the in-situ UV-O_3 treatment and the few-layer TMD thickness. The C-V characteristics demonstrate an approximately constant capacitance for positive gate voltage, corresponding to the HfO_2 gate oxide capacitance, and a decrease in capacitance in the region -2V to -4 V, consistent with depletion of negative charge at the HfO_2/MoS_2 interface. It is noted that the region of surface depletion in the C-V response in Fig. 2c, is consistent with the sub-threshold region in the transfer characteristics in Fig. 2a. The measured accumulation capacitance is 0.76uF/cm^2. Based on cross section TEM images, the HfO_2 is 13nm, and assuming a k value of 17 for ALD grown HfO_2, this would yield a maximum capacitance value of 1.1uF/cm^2. The lower value obtained experimentally, suggests the possibility of a lower k value interface transition region between the HfO_2 and the MoS_2 which is not immediately obvious from the TEM analysis.

In the capacitance-voltage response in the region -4 V to -2 V, a frequency-dependent distortion (“hump”) in the depletion region is observed, which is consistent with an electrically activated trap response at the high-*k*/MoS_2 interface region. In conventional Si MOSFETs with either SiO_2 or high-*k* oxides, this “hump” is usually attributed to interface traps which exhibit a peak density at a specific energy in the bandgap [36,37], and usually a forming gas anneal around 400°C can passivate the defects [38,39], which are primarily silicon dangling bond (P_b) defects. The C-V response of Si control sample under the same ALD condition was reported in our previous work [28]. HfO_2 formed at low temperature (200°C), without any higher temperature annealing in N_2 or H_2/N_2 can exhibit gap states which result in C-V hysteresis, interface defect response, and lower than expected dielectric constant. However, the HfO_2/Si control sample will not be representative of the HfO_2/MoS_2 interface due to the different substrate material and interfacial condition. (e.g. The Si substrate surface will spontaneously form a SiO_2-like interfacial layer during an ALD process, which primarily determines the interfacial property of the HfO_2/Si [40]). Published C-V frequency dependence data on a metal / (30nm) HfO_2 / monolayer MoS_2 gate stack was reported by Zhu et al. [18], where chemical vapor deposited (CVD) MoS_2 was utilized in the device structure. Compared with the device based on CVD MoS_2, this gate stack with mechanically exfoliated MoS_2 shows much less frequency dispersion, suggesting significantly fewer interface defects. A limited study of the C-V frequency dependence on semi-bulk MoS_2 with Al_2O_3 has also been reported [31], where interface defects (D_{it}) ranging from 10^{11} $cm^{-2}eV^{-1}$ to 10^{14} $cm^{-2}eV^{-1}$ were reported. However, the lateral shift of C-V curves possibly convoluted positive oxide charge with interface defects in the D_{it} extraction process.

The techniques that we are about to describe to analyze the D_{it} are only valid when the device is not fully depleted, which must be carefully adhered to when using very thin flakes. In this work, the flake is not fully depleted over the bias range where the D_{it} response is detected. If the MoS_2 thin film is fully depleted, the capacitance should be 0 F (or at a constant number over a voltage range due to parasitic capacitance components) [41]. As shown in Fig. 3a, at about -3V where interface traps are detected, the transistor is not fully turned off (i.e., not fully depleted and still has carriers in the flake responding to the AC signal). Further evidence, based on series resistance analysis (supporting information Fig. S1, S2), confirms that the device is not fully depleted in the V_g range used to analyze the D_{it} from the multi-frequency C-V measurements. Due to the influence of the interface traps, the inverse subthreshold slope (SS) also increases at around -3V. This change of SS is also consistent with the charging of MoS_2/HfO_2 interface traps providing an independent measurement technique indicating that the C-V response is detecting interface traps at the corresponding region of the C-V response. SS can be used to roughly estimate D_{it} since $SS = 60mV \cdot [1+(C_{dm}+C_{it})/C_{ox}]$, where C_{dm} is the capacitance of depleted MoS_2 and C_{it} is the capacitance due to interface traps. Thus, C_{it} and D_{it} (C_{it}/q) can be estimated by comparing the change in SS around -3.8 V (110 mV/dec) and around -3.2 V (318 mV/dec). The calculated result gives $D_{it} = 1.6\times10^{13}$ cm^{-2} eV^{-1}.

Next, we quantified the D_{it} from the C-V response (Fig. 2c). As the frequency is increased from 1 kHz to 500 kHz, this reduces the AC response of the interface defects to the measured capacitance, resulting in the dispersion of capacitance with frequency noted in the region from -2.5 V to -3.5 V in Fig. 2c. In the limit of increasing frequency, the interface defects will only respond to the DC bias (high frequency D_{it} response), and the interface states will be evident as a “plateau” region of the C-V in the case where the interface states are located in a narrow band of energies. From Fig. 2c, at frequencies above 100 kHz, an approximate plateau region is observed. At 500 kHz this region extends from -2.8 V and -3.4 V. We interpret this 0.6V gate voltage region to be due to the DC response of the defects [42]. This is illustrated in schematic energy band diagrams in Fig. 3b, with surface Fermi level pinning due to interface states with a peak density in a specific energy in the band gap[(1)]. The total density of interface defects, in the areal density units of cm^{-2}, can be estimated from the oxide capacitance and the width of the plateau region in the 500kHz CV response, and this yields an interface trap density $D_{it} = 2.7\times10^{12}\ cm^{-2}$. A more detailed calculation is shown in the supporting information S.3. Although the possibility that the defects still respond with AC signal at 500kHz could not be fully excluded, an abrupt C-V distortion due to peaked distribution of interface defects[42] is consistent with our following D_{it} extraction and analysis.



[(1)] The plateau region is not a constant capacitance. This would only occur for a mono-energetic defect level at a temperature of zero K.

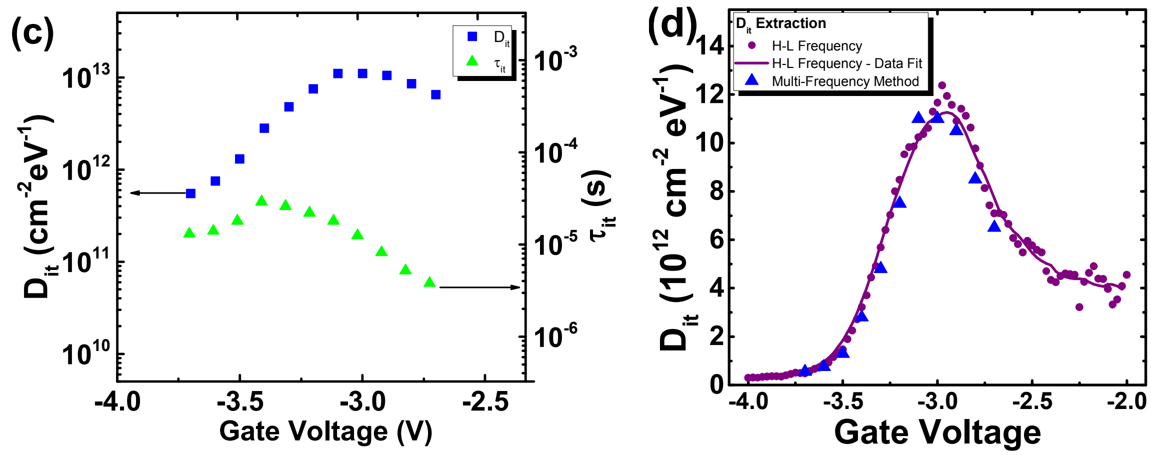


Figure 4. D_{it} extraction. (a) D_{it} vs V_{GS}, calculated by High-Low Frequency method; (b) Re-plotted "Capacitance vs Voltage" to "Capacitance vs Frequency" (dots), and modeling (solid lines); (c) D_{it} vs V_{GS} and τ_{it} vs V_{GS}, from the modeling work in (b); (d) Comparison of two D_{it} extraction methods in (a) and (c), showing similar D_{it} distribution, with a D_{it} peak at 1.2×10^{13} cm^{-2} eV^{-1}.

Fig. 4a shows the D_{it} calculated by the conventional high-low frequency method [42] from equations

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \quad (1)$$

$$D_{it} = C_{it}/q \quad (2)$$

where capacitance of interface traps (C_{it}) represents the capacitance when all the traps reacted with AC signal at low frequency; C_{LF} and C_{HF} are the capacitance measured at 1 kHz and 500 kHz respectively. In Fig. 4a, the polynomial function is a guide to the eye. D_{it} ranges from the order of 10^{12} to 10^{13} cm^{-2} eV^{-1}, with a peak value of 1.2×10^{13} cm^{-2} eV^{-1}. The peak value is one order of magnitude lower than what was reported in reference [31] using the same high-low frequency method, and aluminum oxide as the dielectric. It is in the same range as the defect density in literature for exfoliated MoS_2 by photo-excited charge collection spectroscopy [43]. Translating each gate voltage in Fig. 4a to a corresponding surface potential at the MoS_2/HfO_2

interface, requires a known value of the active *n*-type doping concentration in the MoS_2. This value is not readily known for the geological samples employed here, and as a consequence, the D_{it} versus energy in the MoS_2 energy gap cannot be determined for these devices.

An alternative method was also employed to extract D_{it} [18]. Instead of only using the C-V data of high and low frequencies, data from the complete span of frequencies was used, and using this approach both D_{it} and the trap time constant τ_{it} can be extracted. (The importance of τ_{it} is that one can extract the trap cross section, σ, and trap energy, E_T, with temperature dependent experiments [33] to understand the physical origin of the interface traps, and this is beyond the scope of this work.) In this multi-frequency method, C_{it} is determined by D_{it} and τ_{it} at certain voltages.

$$C_{it} = \frac{qD_{it}}{1+\omega^2\tau_{it}^2} \quad (3)$$

where $\omega=2\pi f$, and f is the applied AC frequency. Thus, at certain voltages, D_{it} and τ_{it} can be extracted from the C-f or C-ω relationship. Fig. 4b shows the measured data (symbols) and model fit (lines) for the capacitance versus frequency for the voltage range corresponding to the interface defects response in the C-V characteristic. From Fig. 4b, the values of D_{it}, and the corresponding τ_{it} values, can be determined at each gate voltage, and the characteristics are shown in Fig. 4c. The two methods are compared in Fig. 4d, demonstrating consistency between the two D_{it} extraction approaches. Detailed modeling work for these two methods can be found in S.3 and S.4.

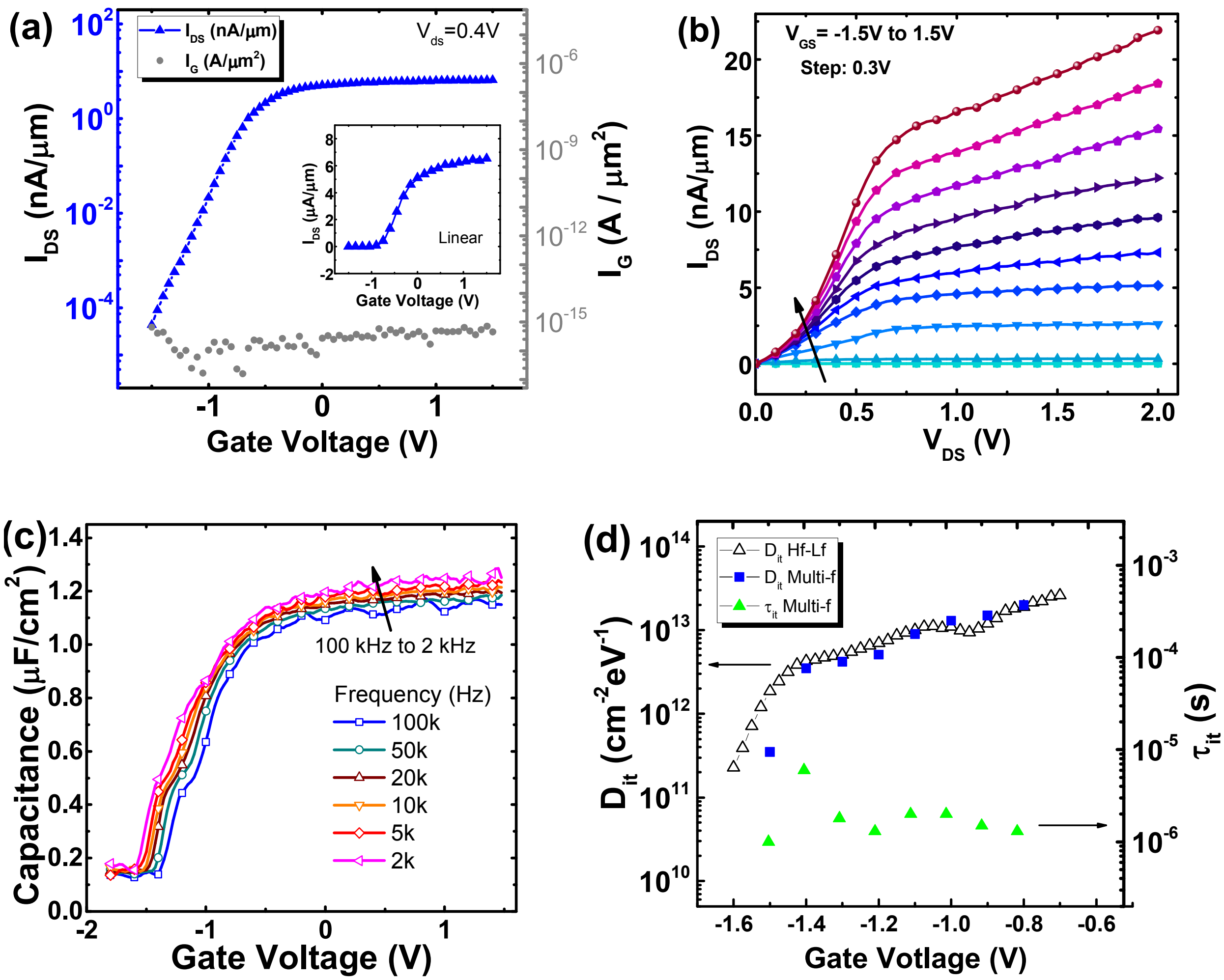


Figure 5. Electrical characterization and D_{it} extraction of a device with 8 nm HfO_2 and 4-layer MoS_2. (W=7.2µm, L=5.6µm) (a) I_{DS} - V_{GS} and gate leakage; (b) Corresponding I_{DS}-V_{DS}; (c) C-V: frequency dependence; C-V curves disperse in the entire depletion voltage range, indicating interface traps in range of energy levels; (d) D_{it} vs V_{GS} and τ_{it} vs V_{GS}, D_{it} ranges from 2×10^{11} cm^{-2} eV^{-1} to 2×10^{13} cm^{-2} eV^{-1}, with both H-L frequency method and multi-frequency method.

Due to possible variation in the electronic properties of exfoliated MoS_2 flakes for differing samples, and within a given crystal, in addition to contaminants and the presence of surface defects [44], we applied the same methods on a different MoS_2 transistor with 8nm HfO_2 and a 4-layer MoS_2 flake to verify if the C-V analysis method is more broadly applicable. Fig. 5a and 5b shows the I_{DS}-V_{GS}, gate leakage and I_{DS}-V_{DS} characteristics of this transistor. The gated area is width × length = 7.2 μm × 5.6 μm. Fig. 5c and 5d shows the C-V frequency dependence, along with the extracted D_{it} with two methods. The C-V frequency dispersion (Fig. 5c) suggests a different distribution of interface defects at the HfO_2/MoS_2 interface compared to the sample analyzed in Fig. 4. The frequency dependent C-V characteristics are consistent with an interface state density distributed throughout the MoS_2 energy gap at the HfO_2/MoS_2 interface. Fig. 5d shows the D_{it} and τ_{it} extracted using high-low frequency and multi-frequency methods. The magnitude of D_{it} and τ_{it} are comparable to the 7-layer MoS_2 flake MOSFET shown in Fig. 4, but in this case no peak in D_{it} is evident. Similar variation has also been reported in other publications using thicker MoS_2 layers [33], and the variation from sample to sample (with nominally identical processing) is also manifest in the transport properties [32]. This variability in interface and transport properties is most likely a consequence of the high density and variability of impurities and defects in both geological and grown MoS_2.[44,45]

Interfacial sulfur vacancies [46,47] and other types of surface structural defects[48] are the defects often observed by researchers, and can potentially generate these defect responses in the impedance measurement. One possible suggestion for the defect level which shows a peak response at a specific energy in the band gap (Fig. 4), is that the defect results from sulfur vacancies [33], which is reported to have an energy level of 0.35eV from mid gap, from measurements [46]. The alternative behavior of an almost constant D_{it} across the energy gap (Fig. 5), observed in this work and in literature [33], could be a consequence of the area of the certain devices not containing S vacancies within the gate area probed. Both cases (peaked D_{it} & uniform D_{it}) were also reported in Ref 33, showing C-V response of MOS capacitors on semi-bulk MoS_2 flakes, indicating that the samples that we report in this work are representative. We also suspect that the defect response observed in our devices can potentially originate from other impurities and defects present in the flake source [44,45] (i.e., the exfoliated MoS_2 crystal), which can exhibit equivalent surface density values in the range $1x10^{12}$ to $1x10^{13}$ cm^{-2}. In addition, it is possible that the response could originate from defects located in an interfacial transition region between the MoS_2 and the HfO_2 [49–51] because this methodology can also capture border trap response. This is also the subject of on-going studies.

This work provides a relatively easy fabrication procedure and robust electrical characterization methodology to study top-gated metal / high-*k* / TMD devices. The multi-frequency C-V response of the structure is consistent with the existence of electrically active defects at the interface between high-*k* and MoS_2. By combining with simulation and other physical characterization, a route to understand and passivate electrically active interface defects in high-*k* gate TMD MOSFETs is possible .

Conclusion

In conclusion, we designed and photolithographically fabricated top-gated FETs on exfoliated, few-layer MoS_2 flakes, with an in-situ UV-ozone functionalization treatment and 8nm to 13nm ALD HfO_2 dielectrics. Both the transistor performance and the gate-stack interface properties were characterized electrically. Based on impedance spectroscopy of the HfO_2/MoS_2 gate stack in the MOSFET structure, D_{it} was extracted from the frequency dependence of the C-V response using two different methods. The interface state density values were in the range 1×10^{12} to 1×10^{13} cm^{-2} eV^{-1} for the devices studied, with trapping time constants in the range $1x10^{-5}$ to

$1x10^{-6}$ s. One device with 7-L MoS_2 and 13 nm HfO_2 as the gate oxide exhibited a C-V response consistent with a D_{it} distribution peaking at a value of 1.2×10^{13} cm^{-2} eV^{-1} at a specific energy in the MoS_2 band gap. A second device with 4-L MoS_2 and 8 nm HfO_2 yielded D_{it} values ranged from 2×10^{11} cm^{-2} eV^{-1} to 2×10^{13} cm^{-2} eV^{-1} with no peak value of D_{it} observed. The device performance and interface properties indicate that the UV-ozone functionalization is promising for MoS_2-based devices with high-*k* dielectrics to achieve low leakage, thin and continuous high-*k* oxide layers, with interface state density values which allow modulation of the Fermi level at the HfO_2/MoS_2 interface. The relatively simple MOSFET test structure, combined with the gate to channel C-V response, indicates the existence of specific electrically active HfO_2/MoS_2 interface defects , and combining these results with simulation and other physical characterization methods, will provide an increased understanding of the physical origin of defects, as well as a method to monitor the impact of different high-*k* oxides and varying surface preparations on the interface state density at high-*k*/MoS_2 interfaces.

Supporting Information

Proposed equivalent circuits of C-V characterization; Series resistance analysis and full depletion of MoS_2 flake; Number of interface defects (N_{it}) extraction from C-V curves; Defects density (D_{it}) calculation by high-low frequency method; D_{it} and traps time constant τ_{it} extraction by multi-frequency method.

Corresponding Author

*E-mail: chadwin.young@utdallas.edu

Acknowledgment

This work is funded by NSF UNITE US/Ireland R&D Partnership for support under NSF-ECCS–1407765, and Science Foundation Ireland under the US-Ireland R&D Partnership Programme Grant Number SFI/13/US/I2862.

References

(1) Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S. Electronics and Optoelectronics of Two-Dimensional Transition Metal Dichalcogenides. *Nat. Nanotechnol.* **2012**, *7*, 699–712.

(2) Butler, S. Z.; Hollen, S. M.; Cao, L.; Cui, Y.; Gupta, J. A.; Gutiérrez, H. R.; Heinz, T. F.; Hong, S. S.; Huang, J.; Ismach, A. F.; Johnston-Halperin, E.; Kuno, M.; Plashnitsa, V. V.; Robinson, R. D.; Ruoff, R. S.; Salahuddin, S.; Shan, J.; Shi, L.; Spencer, M. G.; Terrones, M.; Windl, W.; Goldberger, J. E. Progress, Challenges, and Opportunities in Two-Dimensional Materials Beyond Graphene. *ACS Nano* **2013**, *7*, 2898–2926.

(3) Fiori, G.; Bonaccorso, F.; Iannaccone, G.; Palacios, T.; Neumaier, D.; Seabaugh, A.; Banerjee, S. K.; Colombo, L. Electronics Based on Two-Dimensional Materials. *Nat. Nanotechnol.* **2014**, *9*, 768–779.

(4) Radisavljevic, B.; Kis, A. Mobility Engineering and a Metal-Insulator Transition in Monolayer MoS□. *Nat. Mater.* **2013**, *12*, 815–820.

(5) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150.

(6) Fuhrer, M. S.; Hone, J. Measurement of Mobility in Dual-Gated MoS2 Transistors. *Nat. Nanotechnol.* **2013**, *8*, 146–147.

(7) Kaasbjerg, K.; Thygesen, K. S.; Jacobsen, K. W. Phonon-Limited Mobility in N-Type Single-Layer MoS 2 from First Principles. *Phys. Rev. B - Condens. Matter Mater. Phys.* **2012**, *85*, 1–16.

(8) Das, S.; Chen, H. Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS2 Transistors with Scandium Contacts. *Nano Lett.* **2013**, *13*, 100–105.

(9) Das, S.; Appenzeller, J. Where Does the Current Flow in Two-Dimensional Layered Systems? *Nano Lett.* **2013**, *13*, 3396–3402.

(10) Kim, S.; Konar, A.; Hwang, W.-S.; Lee, J. H.; Lee, J.; Yang, J.; Jung, C.; Kim, H.; Yoo, J.-B.; Choi, J.-Y.; Jin, Y. W.; Lee, S. Y.; Jena, D.; Choi, W.; Kim, K. High-Mobility and Low-Power Thin-Film Transistors Based on Multilayer MoS2 Crystals. *Nat. Commun.* **2012**, *3*, 1011.

(11) Liu, H.; Ye, P. D. MoS 2 Dual-Gate MOSFET with Atomic-Layer-Deposited Al 2O 3 as Top-Gate Dielectric. *IEEE Electron Device Lett.* **2012**, *33*, 546–548.

(12) Ganatra, R.; Zhang, Q. Few-Layer MoS2: A Promising Layered Semiconductor. *ACS Nano* **2014**, *8*, 4074–4099.

(13) Ruppert, C.; Aslan, O. B.; Heinz, T. F. Optical Properties and Band Gap of Single- and Few-Layer MoTe2 Crystals. *Nano Lett.* **2014**, *14*, 6231–6236.

(14) Pradhan, N. R.; Rhodes, D.; Feng, S.; Xin, Y.; Memaran, S.; Moon, B. H.; Terrones, H.; Terrones, M.; Balicas, L. Field-Effect Transistors Based on Few-Layered Alpha-MoTe2. *ACS Nano* **2014**, *8*, 5911–5920.

(15) Cui, Y.; Xin, R.; Yu, Z.; Pan, Y.; Ong, Z.; Wei, X.; Wang, J.; Nan, H.; Ni, Z.; Wu, Y.; Chen, T.; Shi, Y.; Wang, B.; Zhang, G.; Zhang, Y.-W.; Wang, X. High-Performance Monolayer WS 2 Field-Effect Transistors on High-κ Dielectrics. *Adv. Mater.* **2015**, *27*, 5230–5234.

(16) Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A. High-Performance Single Layered WSe2 P-FETs with Chemically Doped Contacts. *Nano Lett.* **2012**, *12*, 3788–3792.

(17) Liu, W.; Kang, J.; Sarkar, D.; Khatami, Y.; Jena, D.; Banerjee, K. Role of Metal Contacts in Designing High-Performance Monolayer N-Type WSe2 Field Effect Transistors. *Nano Lett.* **2013**, *13*, 1983–1990.

(18) Zhu, W.; Low, T.; Lee, Y.-H.; Wang, H.; Farmer, D. B.; Kong, J.; Xia, F.; Avouris, P. Electronic Transport and Device Prospects of Monolayer Molybdenum Disulphide Grown by Chemical Vapour Deposition. *Nat. Commun.* **2014**, *5*, 3087.

(19) Salvatore, G. A.; Münzenrieder, N.; Barraud, C.; Petti, L.; Zysset, C.; Büthe, L.; Ensslin, K.; Tröster, G. Fabrication and Transfer of Flexible Few-Layers MoS2 Thin Film Transistors to Any Arbitrary Substrate. *ACS Nano* **2013**, *7*, 8809–8815.

(20) Jena, D.; Konar, A. Enhancement of Carrier Mobility in Semiconductor Nanostructures by Dielectric Engineering. *Phys. Rev. Lett.* **2007**, *98*, 1–4.

(21) McDonnell, S.; Brennan, B.; Azcatl, A.; Lu, N.; Dong, H.; Buie, C.; Kim, J.; Hinkle, C. L.; Kim, M. J.; Wallace, R. M. HfO2 on MoS2 by Atomic Layer Deposition: Adsorption Mechanisms and Thickness Scalability. *ACS Nano* **2013**, *7*, 10354–10361.

(22) Yang, J.; Kim, S.; Choi, W.; Park, S. H.; Jung, Y.; Cho, M.-H.; Kim, H. Improved Growth Behavior of Atomic-Layer-Deposited High- K Dielectrics on Multilayer MoS 2 by Oxygen Plasma Pretreatment. *ACS Appl. Mater. Interfaces* **2013**, *5*, 4739–4744.

(23) Pezeshki, A.; Hosseini Shokouh, S. H.; Raza, S. R. A.; Kim, J. S.; Min, S.-W.; Shackery, I.; Jun, S. C.; Im, S. Top and Back Gate Molybdenum Disulfide Transistors Coupled for Logic and Photo-Inverter Operation. *J. Mater. Chem. C* **2014**, *2*, 8023–8028.

(24) Zou, X.; Wang, J.; Chiu, C.-H.; Wu, Y.; Xiao, X.; Jiang, C.; Wu, W.-W.; Mai, L.; Chen, T.; Li, J.; Ho, J. C.; Liao, L. Interface Engineering for High-Performance Top-Gated MoS2 Field-Effect Transistors. *Adv. Mater.* **2014**, *26*, 6255–6261.

(25) Yang, W.; Sun, Q.-Q.; Geng, Y.; Chen, L.; Zhou, P.; Ding, S.-J.; Zhang, D. W. The Integration of Sub-10 Nm Gate Oxide on MoS2 with Ultra Low Leakage and Enhanced Mobility. *Sci. Rep.* **2015**, *5*, 11921.

(26) Azcatl, A.; McDonnell, S.; K. C., S.; Peng, X.; Dong, H.; Qin, X.; Addou, R.; Mordi, G. I.; Lu, N.; Kim, J.; Kim, M. J.; Cho, K.; Wallace, R. M. MoS2 Functionalization for Ultra-Thin Atomic Layer Deposited Dielectrics. *Appl. Phys. Lett.* **2014**, *104*, 111601.

(27) Azcatl, A.; KC, S.; Peng, X.; Lu, N.; McDonnell, S.; Qin, X.; de Dios, F.; Addou, R.; Kim, J.; Kim, M. J.; Cho, K.; Wallace, R. M. HfO 2 on UV–O 3 Exposed Transition Metal Dichalcogenides: Interfacial Reactions Study. *2D Mater.* **2015**, *2*, 14004.

(28) Zhao, P.; Vyas, P. B.; McDonnell, S.; Bolshakov-Barrett, P.; Azcatl, A.; Hinkle, C. L.; Hurley, P. K.; Wallace, R. M.; Young, C. D. Electrical Characterization of Top-Gated Molybdenum Disulfide Metal–oxide–semiconductor Capacitors with High-K Dielectrics. *Microelectron. Eng.* **2015**, *147*, 151–154.

(29) Liu, H.; Si, M.; Deng, Y.; Neal, A. T.; Du, Y.; Najmaei, S.; Ajayan, P. M.; Lou, J.; Ye, P. D. Switching Mechanism in Single-Layer Molybdenum Disulfide Transistors: An Insight into Current Flow across Schottky Barriers. *ACS Nano* **2014**, *8*, 1031–1038.

(30) Liu, W.; Sarkar, D.; Kang, J.; Cao, W.; Banerjee, K. Impact of Contact on the Operation and Performance of Back-Gated Monolayer MoS 2 Field-Effect-Transistors. *ACS Nano* **2015**, *9*, 7904–7912.

(31) Park, S.; Kim, S. Y.; Choi, Y.; Kim, M.; Shin, H.; Kim, J.; Choi, W. Interface Properties of Atomic-Layer-Deposited Al 2 O 3 Thin Films on Ultraviolet/Ozone-Treated Multilayer MoS 2 Crystals. *ACS Appl. Mater. Interfaces* **2016**, *8*, 11189–11193.

(32) Mori, T.; Ninomiya, N.; Kubo, T.; Uchida, N.; Watanabe, E.; Tsuya, D.; Moriyama, S.; Tanaka, M.; Ando, A. Characterization of Effective Mobility and Its Degradation Mechanism in MoS 2 MOSFETs. *IEEE Trans. Nanotechnol.* **2016**, *15*, 651–656.

(33) Takenaka, M.; Ozawa, Y.; Han, J.; Takagi, S. Quantitative Evaluation of Energy Distribution of Interface Trap Density at MoS 2 MOS Interfaces by the Terman Method. *IEEE Int. Electron Devices Meet.* **2016**, 139–142.

(34) Wang, F.; Stepanov, P.; Gray, M.; Ning Lau, C. Annealing and Transport Studies of Suspended Molybdenum Disulfide Devices. *Nanotechnology* **2015**, *26*, 105709.

(35) Mirabelli, G.; Schmidt, M.; Sheehan, B.; Cherkaoui, K.; Monaghan, S.; Povey, I.; McCarthy, M.; Bell, A. P.; Nagle, R.; Crupi, F.; Hurley, P. K.; Duffy, R. Back-Gated Nb-Doped MoS2 Junctionless Field-Effect-Transistors. *AIP Adv.* **2016**, *6*, 25323.

(36) Cartier, E.; Stathis, J. H. Hot-Electron Induced Passivation of Silicon Dangling Bonds at the Si(111)/SiO2 Interface. *Appl. Phys. Lett.* **1996**, *69*, 103.

(37) O'Sullivan, B. J.; Hurley, P. K.; Leveugle, C.; Das, J. H. Si(100)-SiO2 Interface Properties Following Rapid

Thermal Processing. *J. Appl. Phys.* **2001**, *89*, 3811–3820.

(38) Carter, R. J.; Cartier, E.; Kerber, A.; Pantisano, L.; Schram, T.; De Gendt, S.; Heyns, M. Passivation and Interface State Density of SiO[sub 2]/HfO[sub 2]-Based/polycrystalline-Si Gate Stacks. *Appl. Phys. Lett.* **2003**, *83*, 533.

(39) Hurley, P. K.; Cherkaoui, K.; O'Connor, E.; Lemme, M. C.; Gottlob, H. D. B.; Schmidt, M.; Hall, S.; Lu, Y.; Buiu, O.; Raeissi, B.; Piscator, J.; Engstrom, O.; Newcomb, S. B. Interface Defects in HfO2, LaSiOx, and Gd2O3 High-k/Metal–Gate Structures on Silicon. *J. Electrochem. Soc.* **2008**, *155*, G13–G20.

(40) Bersuker, G.; Park, C. S.; Barnett, J.; Lysaght, P. S.; Kirsch, P. D.; Young, C. D.; Choi, R.; Lee, B. H.; Foran, B.; van Benthem, K.; Pennycook, S. J.; Lenahan, P. M.; Ryan, J. T. The Effect of Interfacial Layer Properties on the Performance of Hf-Based Gate Stack Devices. *J. Appl. Phys.* **2006**, *100*, 94108.

(41) Chen, J.; Solomon, R.; Chan, T.-Y.; Ko, P.-K.; Hu, C. A CV Technique for Measuring Thin SOI Film Thickness. *IEEE Electron Device Lett.* **1991**, *12*, 453–455.

(42) Schroder, D. K. *Semiconductor Material and Device Characterization*; John Wiley & Sons, Inc.: Hoboken, NJ, USA, 2005.

(43) Choi, K.; Raza, S. R. A.; Lee, H. S.; Jeon, P. J.; Pezeshki, A.; Min, S.-W.; Kim, J. S.; Yoon, W.; Ju, S.-Y.; Lee, K.; Im, S. Trap Density Probing on Top-Gate MoS□ Nanosheet Field-Effect Transistors by Photo-Excited Charge Collection Spectroscopy. *Nanoscale* **2015**, *7*, 5617–5623.

(44) Addou, R.; McDonnell, S.; Barrera, D.; Guo, Z.; Azcatl, A.; Wang, J.; Zhu, H.; Hinkle, C. L.; Quevedo-Lopez, M.; Alshareef, H. N.; Colombo, L.; Hsu, J. W. P.; Wallace, R. M. Impurities and Electronic Property Variations of Natural MoS 2 Crystal Surfaces. *ACS Nano* **2015**, *9*, 9124–9133.

(45) Addou, R.; Colombo, L.; Wallace, R. M. Surface Defects on Natural MoS 2. *ACS Appl. Mater. Interfaces* **2015**, *7*, 11921–11929.

(46) Qiu, H.; Xu, T.; Wang, Z.; Ren, W.; Nan, H.; Ni, Z.; Chen, Q.; Yuan, S.; Miao, F.; Song, F.; Long, G.; Shi, Y.; Sun, L.; Wang, J.; Wang, X. Hopping Transport through Defect-Induced Localized States in Molybdenum Disulphide. *Nat. Commun.* **2013**, *4*, 1–6.

(47) Yu, Z.; Pan, Y.; Shen, Y.; Wang, Z.; Ong, Z.-Y.; Xu, T.; Xin, R.; Pan, L.; Wang, B.; Sun, L.; Wang, J.; Zhang, G.; Zhang, Y. W.; Shi, Y.; Wang, X. Towards Intrinsic Charge Transport in Monolayer Molybdenum Disulfide by Defect and Interface Engineering. *Nat. Commun.* **2014**, *5*, 5290.

(48) Zhou, W.; Zou, X.; Najmaei, S.; Liu, Z.; Shi, Y.; Kong, J.; Lou, J.; Ajayan, P. M.; Yakobson, B. I.; Idrobo, J. C. Intrinsic Structural Defects in Monolayer Molybdenum Disulfide. *Nano Lett.* **2013**, *13*, 2615–2622.

(49) Dolui, K.; Rungger, I.; Sanvito, S. Origin of the N-Type and P-Type Conductivity of MoS2 Monolayers on a SiO2 Substrate. *Phys. Rev. B* **2013**, *87*, 165402.

(50) Ghatak, S.; Pal, A. N.; Ghosh, A. Nature of Electronic States in Atomically Thin MoS2 Field-Effect Transistors. *ACS Nano* **2011**, *5*, 7707–7712.

(51) Lu, C.-P.; Li, G.; Mao, J.; Wang, L.-M.; Andrei, E. Y. Bandgap, Mid-Gap States, and Gating Effects in MoS 2. *Nano Lett.* **2014**, *14*, 4628–4633.

Graphic for Table of Contents (TOC)